ABSTRACT OF THE DISCLOSURE

A twin-cell type semiconductor memory device in which the area of a chip can be reduced. In the twin-cell type semiconductor memory device for storing data in at least one pair of memory cells as complementary information, memory cells are arranged at each of a plurality of word lines at intervals at which bit lines are located. At least the one pair of memory cells, which have stored the complementary information and which indicate a plurality of areas each connected to a pair of bit lines, form a twin cell.